

# z e t e r a

## Zetera White Paper on **Core Logic Embedded $\mu$ SAN<sup>TM</sup>**

*An overview, compare and contrast, technical paper on embedding  $\mu$ SAN<sup>TM</sup> storage into existing computer core logic to give PC's appliance like  $\mu$ SAN<sup>TM</sup> availability and transparently provide the computer with access to the  $\mu$ SAN<sup>TM</sup> storage scalability.*

*This document references the  $\mu$ SAN<sup>TM</sup> (Version .35) and IDE  $\mu$ SAN<sup>TM</sup> (Version .01) White Papers and assumes the reader is familiar with these concepts and protocol.*

Version 0.01

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— *Confidential* —

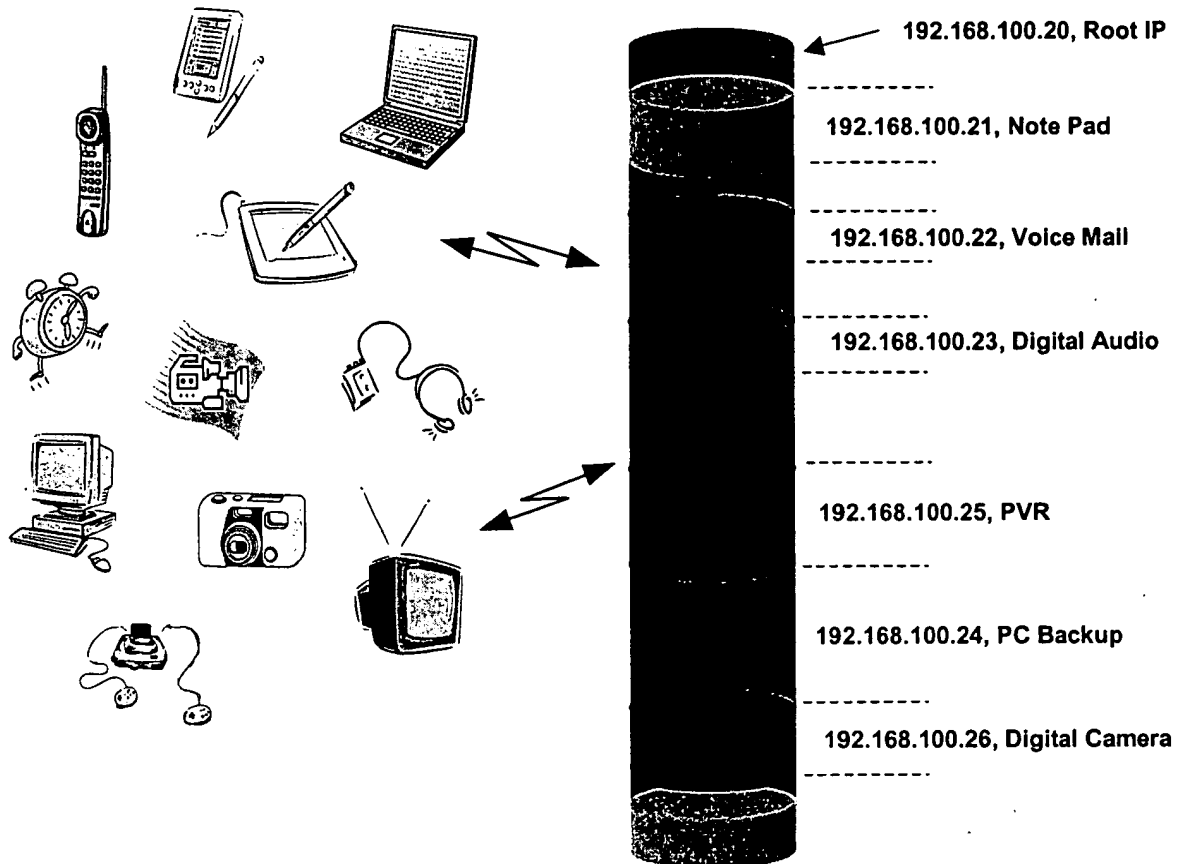
## Revision History

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Original Release

## Overview

The  $\mu$ SAN™ and IDE  $\mu$ SAN™ White Papers identify a storage system, protocol and implementation, which uniquely enable the  $\mu$ SAN™ client protocol into latent PC. This paper describes further extension of those protocols into the future PC space.



This paper identifies one method of transparently integrating both the Client and Storage  $\mu$ SAN™ protocol within the PC's chipset providing several advantages over other implementations including but not limited too:

- Appliance Like  $\mu$ SAN™ Storage availability independent of OS availability.
- Immediate  $\mu$ SAN™ compatibility for any OS supporting industry standard IDE Drivers.
- Immediate OS compatibility with  $\mu$ SAN™ transparent spanning features.
- Immediate OS compatibility with  $\mu$ SAN™ transparent mirroring features.

These unique capabilities are based on the ability of the PC's core logic and BIOS to transparently emulate IDE to the OS while accessing the PC's drive as a  $\mu$ SAN™. Essentially this provides the PC's OS with access to all of the features of a  $\mu$ SAN™ client while maintaining all of the high availability features of a stand alone  $\mu$ SAN™.

This is an extremely low cost, (License + Pennies) way to provide core convergence between the PC and appliances marketed by PC manufacturers penetrating both spaces with a convergence strategy.

Proper implementation of the IDE /  $\mu$ SAN™ emulation within the hardware channel processor eliminates the local OS latency normally associated with such protocol conversions. The unique 1:1 relationship between IDE and  $\mu$ SAN™ LBA make this a trivial acceleration biased toward the local OS and remote QOS.

Figure 1:

